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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/685,599	10/16/2003	Riichiro Shirota	243712US2S DIV	5145

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EXAMINER	
TRAN, THIEN F	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 03/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/685,599	SHIROTA ET AL.	
	Examiner	Art Unit	
	Thien F. Tran	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 February 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *29,31 and 34-47* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *29,34-37 and 42-47* is/are allowed.

6)☒ Claim(s) *31 and 39-41* is/are rejected.

7)☒ Claim(s) *38* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 02/15/2005 has been entered.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 31 and 39-41 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Admitted Prior Art (APA of Figure 8) in view of Yaegashi et al. (USPN 6,265,739).

APA discloses a semiconductor memory device (Figure 8 in the application) comprising a semiconductor substrate 21; a first element isolating insulation film 22 and a second element isolating insulation film 22, for isolating an element region 23, the second element isolating insulation film 22 having a part having a same height as that of the first element isolating insulation film; a first gate electrode 25 including a first portion having a side surface in contact with a side surface of the first element isolating

insulation film and a second portion having a side surface not aligned with the side surface of the first portion of the first gate electrode, the second portion projecting from an upper surface of the first element isolating insulation film; a second gate electrode 27 including a first portion provided on the first gate electrode with a first insulation film 26 interposed therebetween and a second portion extending on the first element isolating insulation film, the second portion having a thickness different from that of the first portion of the second gate electrode; and a resistance element 25a provided on the second element isolating insulation film, the resistance element being formed of a same material as that of the second gate electrode 27 and not extending on the element region. APA does not disclose the side surface of the second portion of the first gate electrode 25 being aligned with the side surface of the first portion of the first gate electrode. Yaegashi et al. discloses the memory cell in Figure 23 having a first gate electrode 106 including a first portion having a side surface in contact with a side surface of the first element isolating insulation film 218 and a second portion having a side surface aligned with the side surface of the first portion of the first gate electrode, the second portion projecting from an upper surface of the first element isolating insulation film 218. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to form the memory cells in the cell section of APA with the memory cell of Yaegashi et al. wherein the side surface of the second portion of the first gate electrode is aligned with the side surface of the first portion of the first gate electrode so that the memory device can be manufactured at low cost.

Regarding claim 39, the second portion of the second gate electrode and the resistance element are isolated from each other on the second element isolating insulation film.

Regarding claim 40, the first gate electrode is a floating gate of a non-volatile semiconductor memory, and the second gate electrode is a control gate electrode.

Regarding claim 41, the resistance element is part of a peripheral control circuit provided on a periphery of a memory cell array region.

Allowable Subject Matter

Claims 29, 34-37 and 42-47 are allowed.

Claim 38 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thien F. Tran whose telephone number is (571) 272-1665. The examiner can normally be reached on 8:30AM - 5:00PM Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

tt
March 6, 2005

Thien Tran

THIEN TRAN
PRIMARY EXAMINER